REMARKS

This responds to the Office Action mailed on June 3, 2004.

Claims 1, 4, 5 and 6 have been amended. No claims have been added or canceled; claims 1, 2, and 4-9 remain pending in this application.

Rejection of Claims Under §102

Claims 1-2 were rejected under 35 USC § 102(b) as being anticipated by Kapustka et al. ("CoSine Communications Moves VPNs 'Into the Cloud' with the Leading Managed IP Service Delivery Platform").

Applicant respectfully traverses the rejection. The section cited by the Examiner as teaching the use of a virtual router to configure the processor elements in the switch is limited to a discussion of the use of virtual routers to connect "Virtual Network Connections" through the service provider's IP or ATM network in order to provide paths "between subscriber locations as well as to the Internet." There is no discussion of how the switch is configured.

In addition, Applicant has amended claim 1 to emphasize the use of objects to control processor elements within the switch. There is no teaching within Kapustka of the use of objects to control processor elements within the switch.

The Examiner stated that Applicant does not specify what a processor element is. Even if this was true, Kapustka still does not describe a system having a plurality of processor elements, where the processor elements are configured as defined and claimed by Applicant.

Reconsideration of claims 1 and 2 is respectfully requested.

Rejection of Claims Under §103

Claims 4-9 were rejected under 35 USC § 103(a) as being unpatentable over Kapustka et al. in view of Alfieri (U.S. 5,745,778).

Kaputska is discussed above.

Alfieri describes a method of assigning threads to processors in a multiprocessor system. Alfieri defines a "thread group" as a set of closely related threads within a process that will tend to access and operate on the same data and suggests that scheduling threads within these groups as a single globally scheduled groups promotes a closer relationship between the threads in the

group and individual processors or groups of processors, thereby improving the ratio of cache hits and overall system performance. Each thread group has attributes that are available to all CPUs in the system. The attributes specify the thread group's allowable CPUs, or set of CPUs and the thread group's minimum allowed processing level.

As noted above, key limitations of claim 1 are missing from Kapustka. These limitations are not taught or suggested by Alfieri. Applicant respectfully requests reconsideration and allowance of claims 4-9.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

ABRAHAM R. MATTHEWS ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date March 8, 2006

By _____
Thomas F. Brennan
Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of March, 2006.

Thomas F. Brennan
Name

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Signature